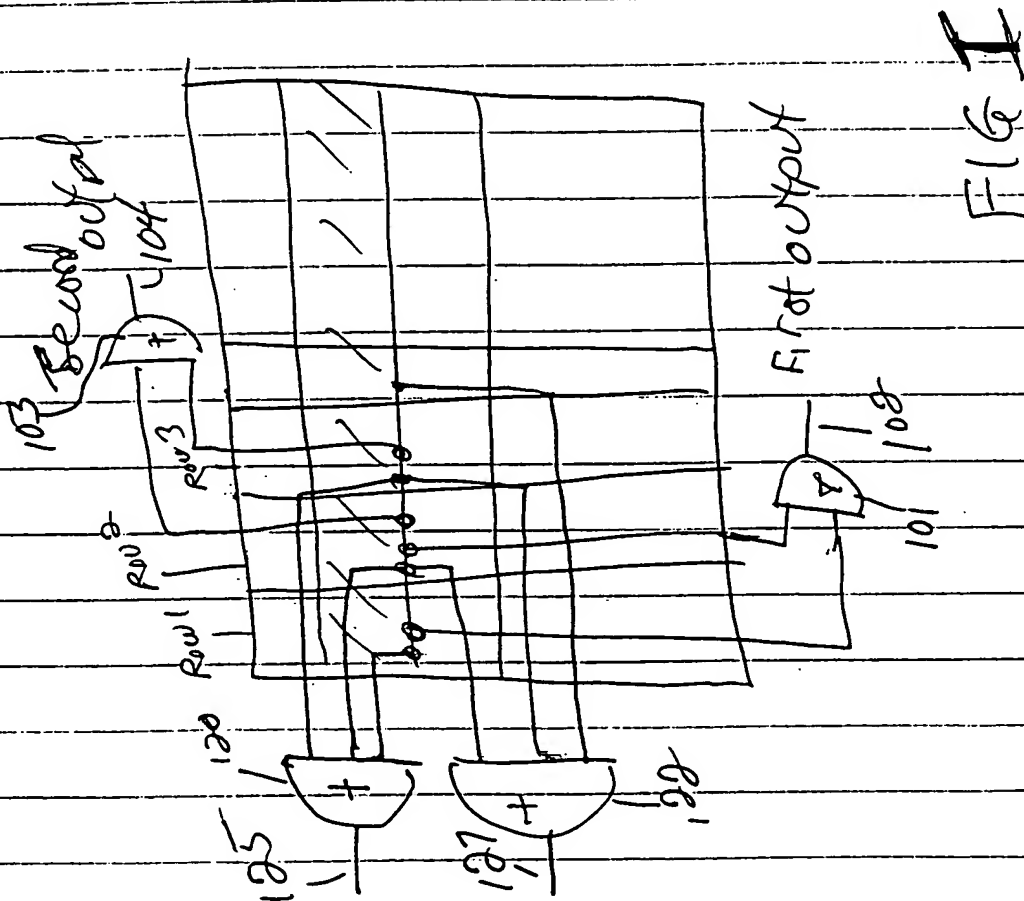
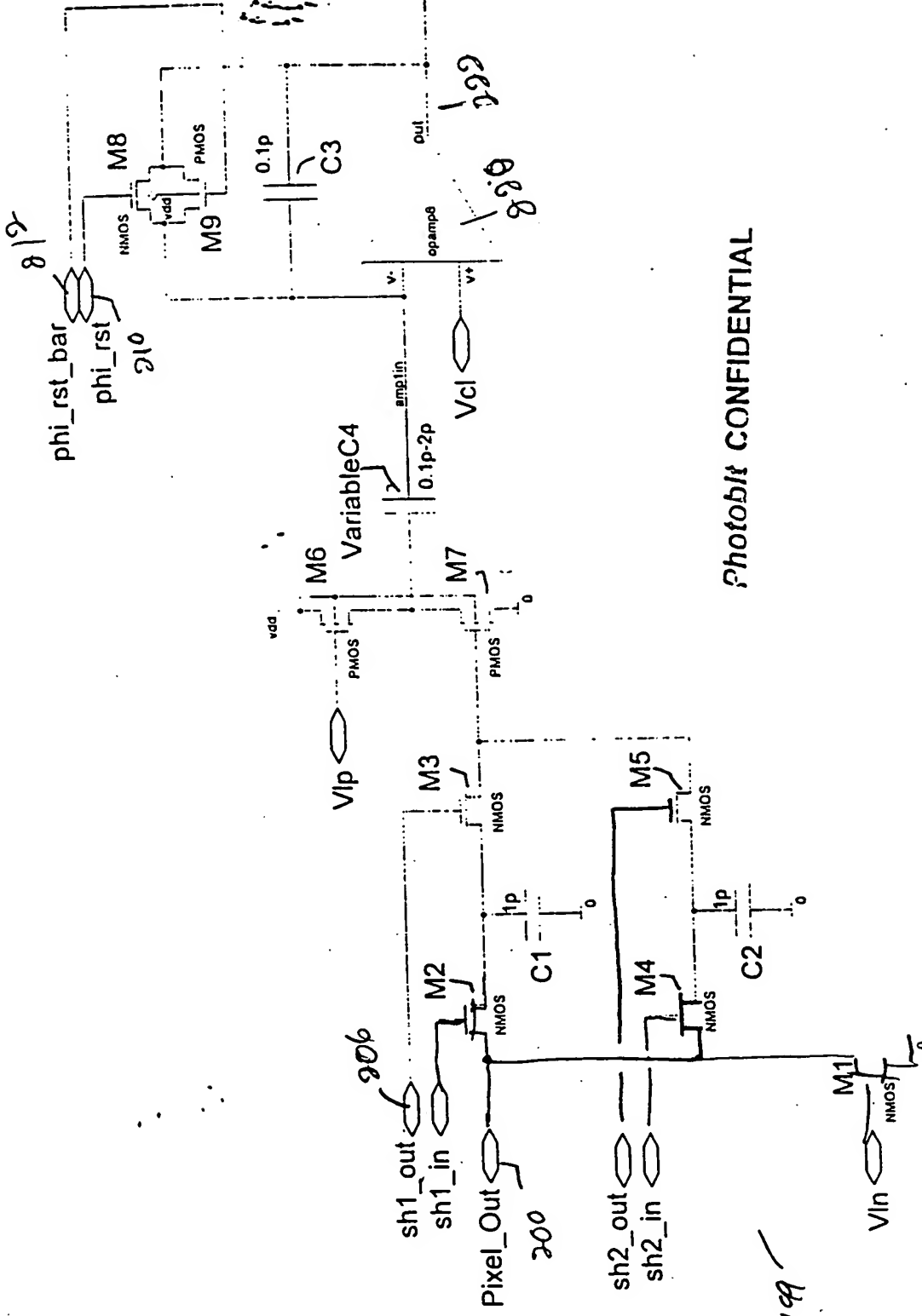


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IMPROVEMENT





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Figure 1a Input/Amplification Stage

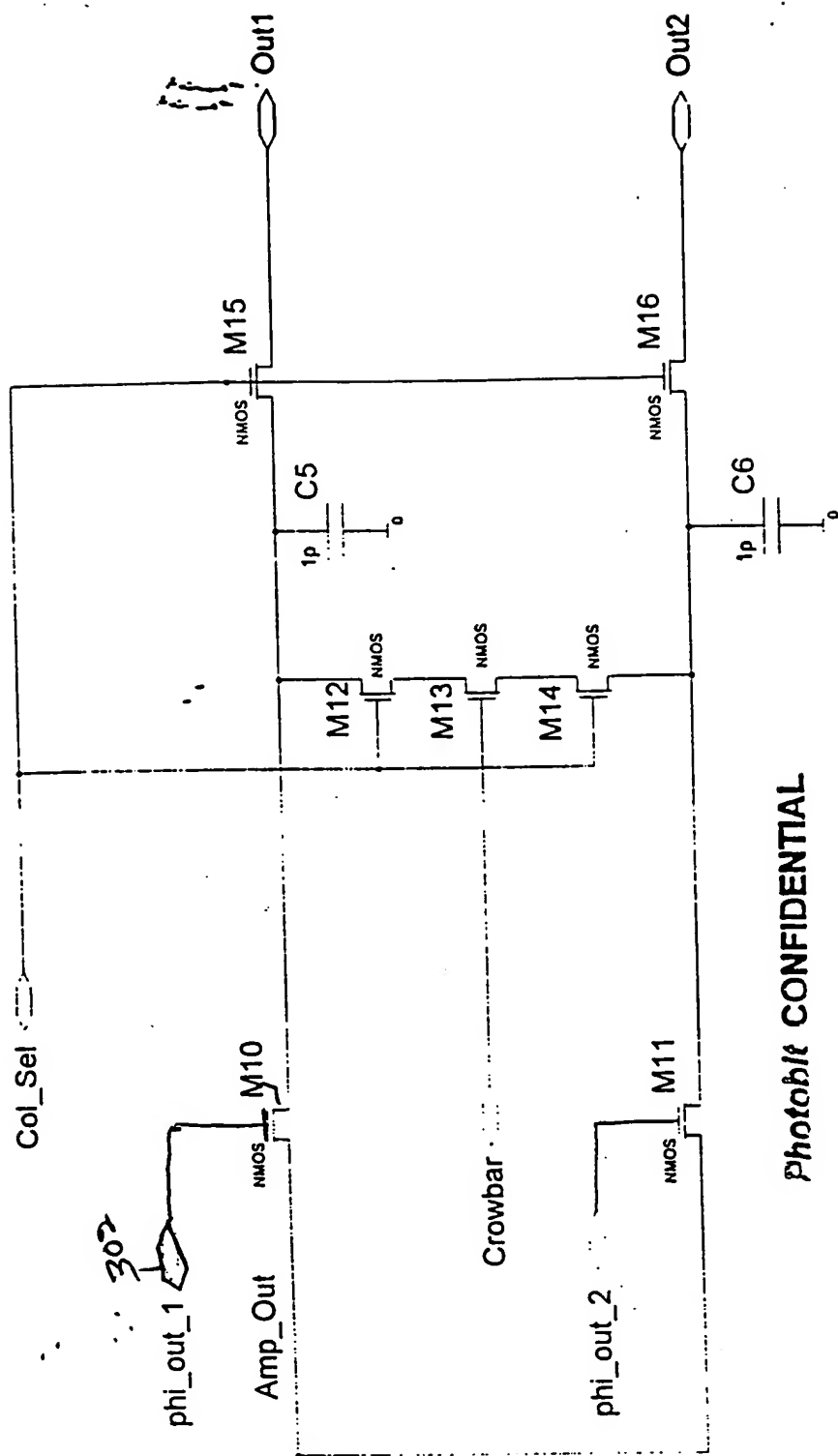


Figure 10: Output/FPN Rejection Stage

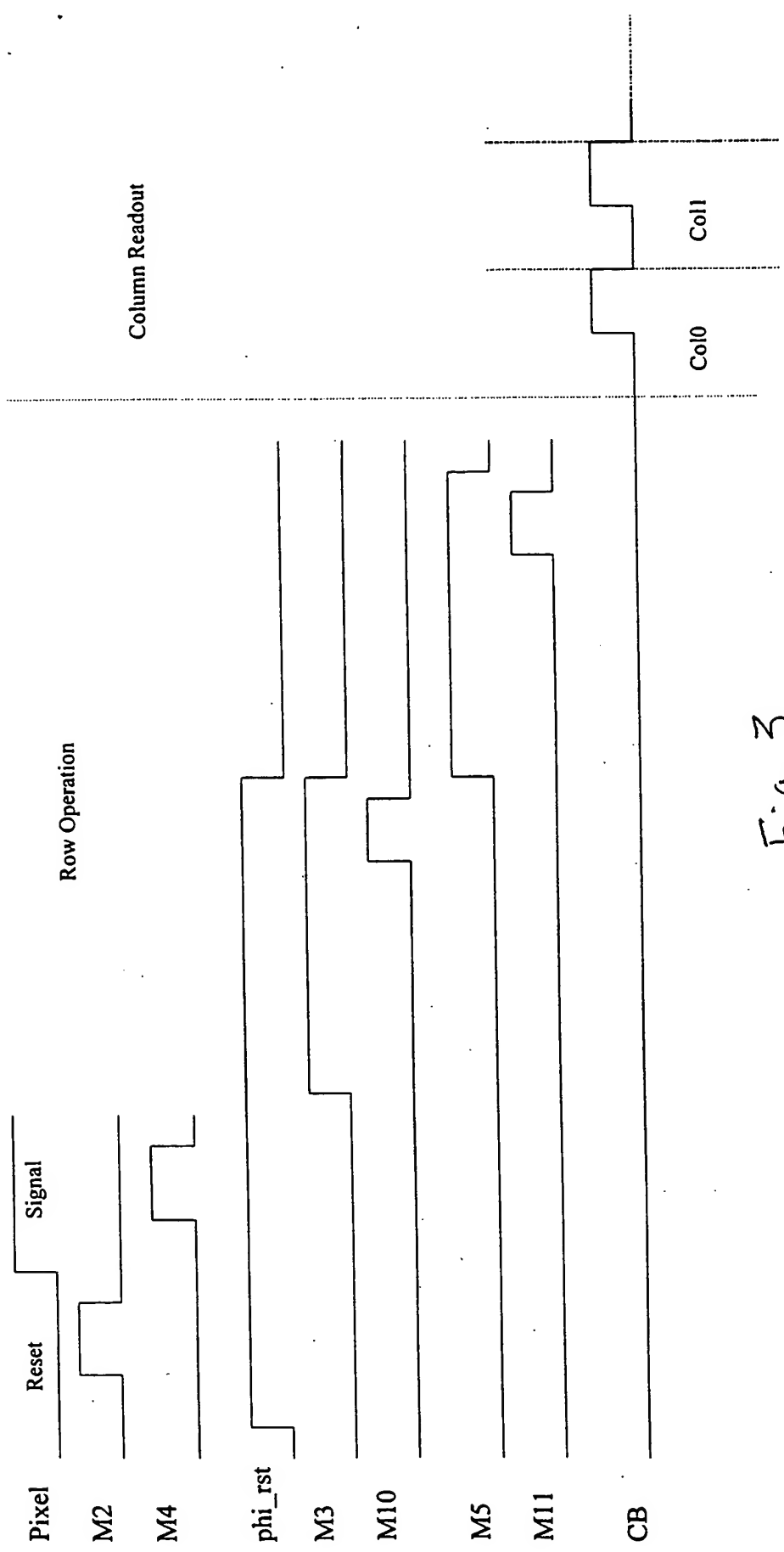


Fig 3

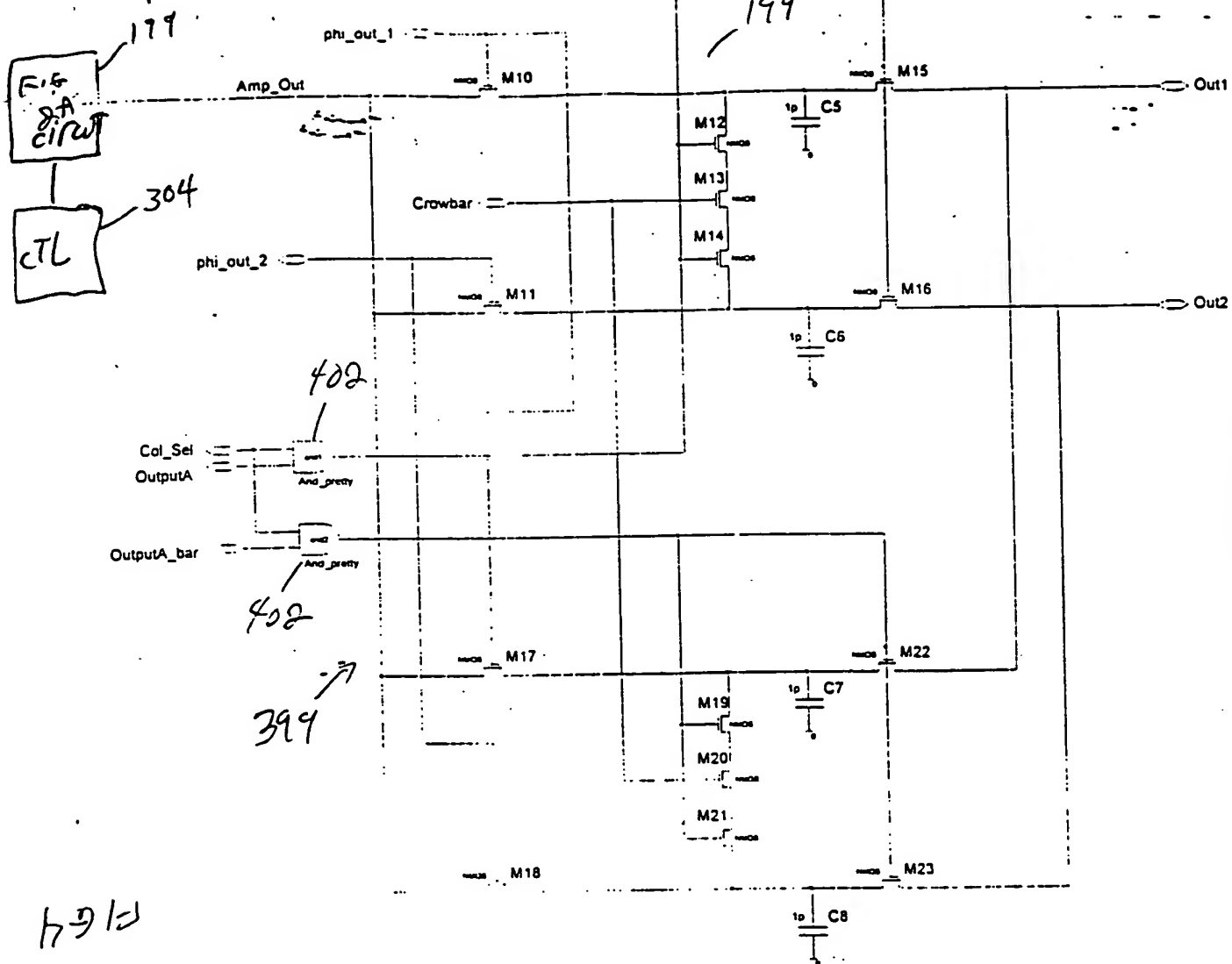


Figure 4: Row Addition Output/FPN Rejection Stage

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